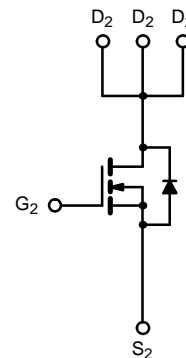
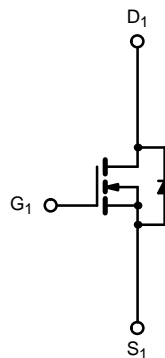
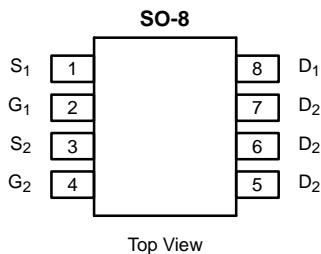




Asymmetric N-Channel, Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel 1	30	0.040 @ $V_{GS} = 10$ V	± 4.7
		0.065 @ $V_{GS} = 4.5$ V	± 3.7
N-Channel 2		0.0175 @ $V_{GS} = 10$ V	± 9
		0.027 @ $V_{GS} = 4.5$ V	± 7.3

**High-Efficiency
PWM Optimized**



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel 1	N-Channel 2	Unit
Drain-Source Voltage	V_{DS}	30	30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^{a, b}	I_D	$T_A = 25^\circ\text{C}$	± 4.7	A
		$T_A = 70^\circ\text{C}$	± 3.7	
Pulsed Drain Current	I_{DM}	± 40	± 60	
Continuous Source Current (Diode Conduction) ^{a, b}	I_S	1.2	2.0	
Maximum Power Dissipation ^{a, b}	P_D	$T_A = 25^\circ\text{C}$	1.4	W
		$T_A = 70^\circ\text{C}$	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	125	90	$^\circ\text{C/W}$	
			$t \leq 10$ sec		
			Steady State		
			N-Ch 2		
Steady State	80				

Notes

- a. Surface Mounted on FR4 Board.
- b. $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit	
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch 1 N-Ch 2	1.0 1.0			V	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	N-Ch 1 N-Ch 2			±100 ±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V	N-Ch 1 N-Ch 2			1 1	μA	
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch 1 N-Ch 2			5 5		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch 1 N-Ch 2	20 30			A	
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.7 A	N-Ch 1		0.033	0.040	Ω	
		V _{GS} = 10 V, I _D = 9 A	N-Ch 2		0.014	0.0175		
		V _{GS} = 4.5 V, I _D = 3.7 A	N-Ch 1		0.048	0.065		
		V _{GS} = 4.5 V, I _D = 7.3 A	N-Ch 2		0.020	0.027		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.7 A	N-Ch 1		12		S	
		V _{DS} = 15 V, I _D = 9 A	N-Ch 2		25			
Diode Forward Voltage ^a	V _{SD}	I _S = 1.2 A, V _{GS} = 0 V	N-Ch 1		0.7	1.2	V	
		I _S = 2.0 A, V _{GS} = 0 V	N-Ch 2		0.7	1.2		
Dynamic^b								
Total Gate Charge	Q _g	N-Channel 1 V _{DS} = 15 V, V _{GS} = 5 V, I _D = 4.7 A N-Channel 2 V _{DS} = 15 V, V _{GS} = 5 V, I _D = 9 A	N-Ch 1 N-Ch 2		6.5 17.5	10 27	nC	
Gate-Source Charge	Q _{gs}		N-Ch 1 N-Ch 2		3.0 7.5			
Gate-Drain Charge	Q _{gd}		N-Ch 1 N-Ch 2		2.5 6.5			
Turn-On Delay Time	t _{d(on)}	N-Channel 1 V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω N-Channel 2 V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω	N-Ch 1 N-Ch 2		10 15	20 30	ns	
Rise Time	t _r		N-Ch 1 N-Ch 2		12 15	20 30		
Turn-Off Delay Time	t _{d(off)}		N-Ch 1 N-Ch 2		20 45	35 70		
Fall Time	t _f		N-Ch 1 N-Ch 2		10 20	20 35		
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.2 A, di/dt = 100 A/μs	N-Ch 1		40		80
			I _F = 2.0 A, di/dt = 100 A/μs	N-Ch 2		40		80

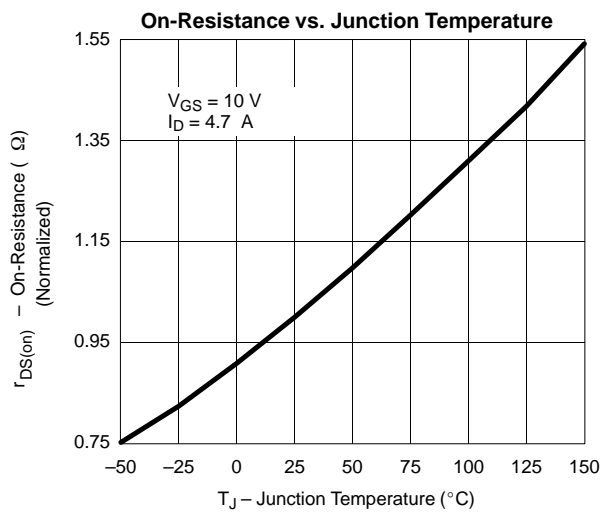
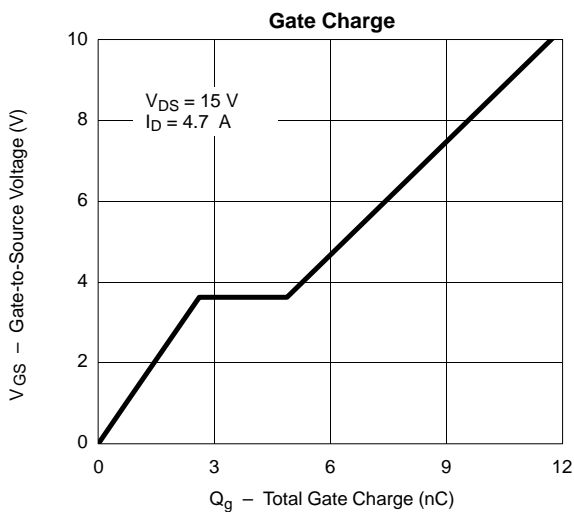
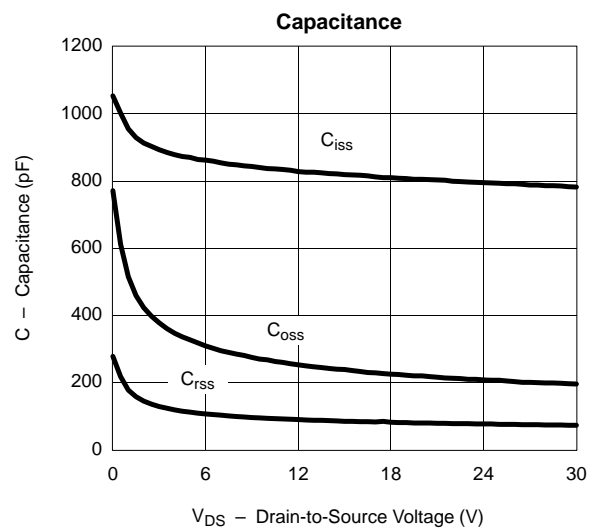
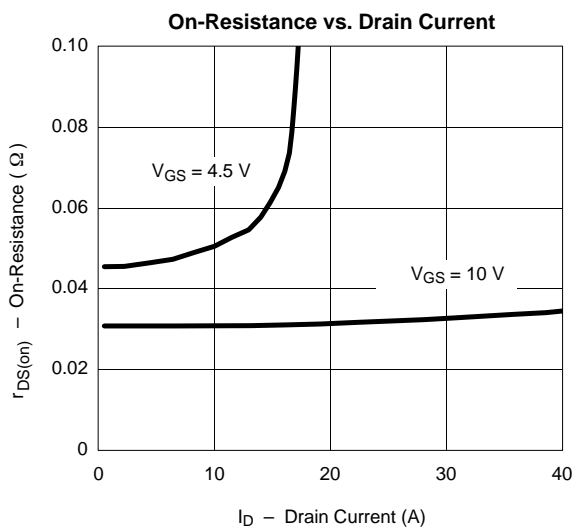
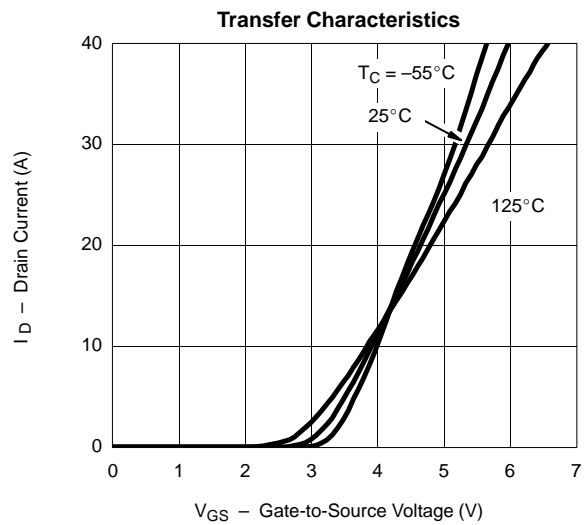
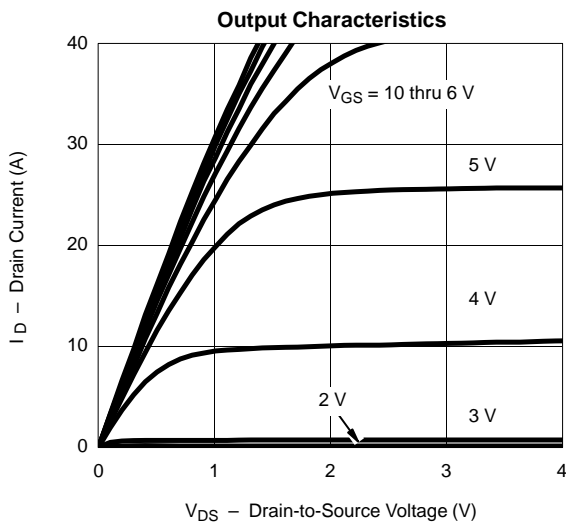
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. For design aid only; not subject to production testing.

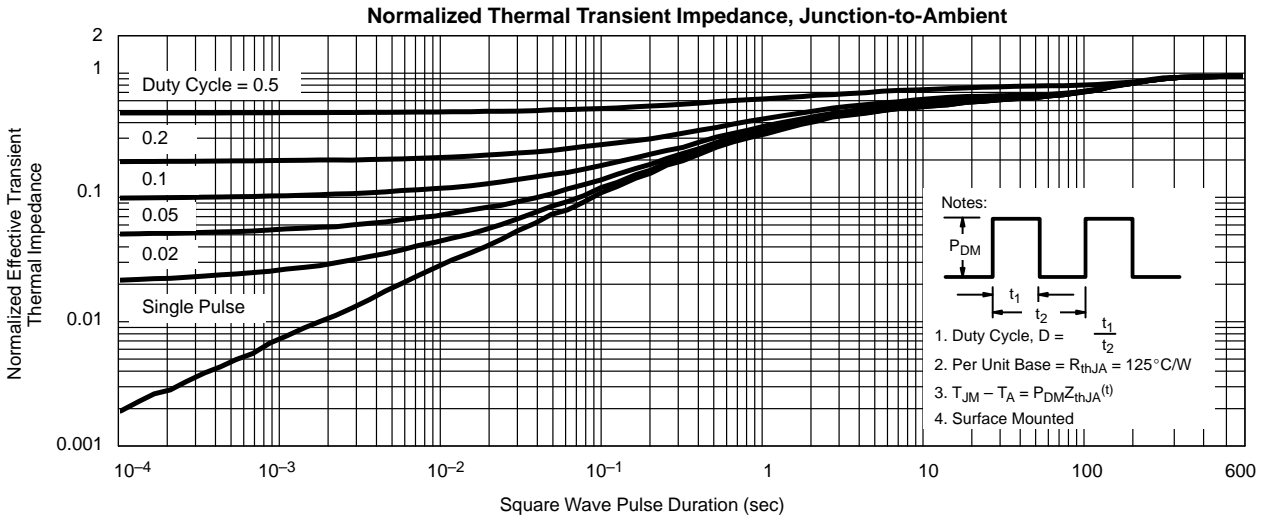
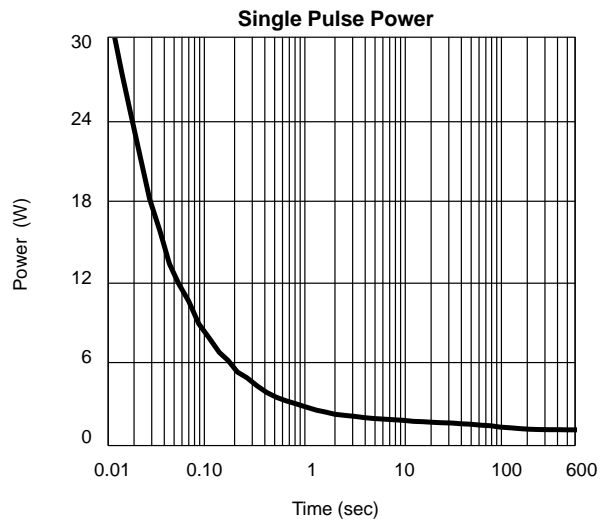
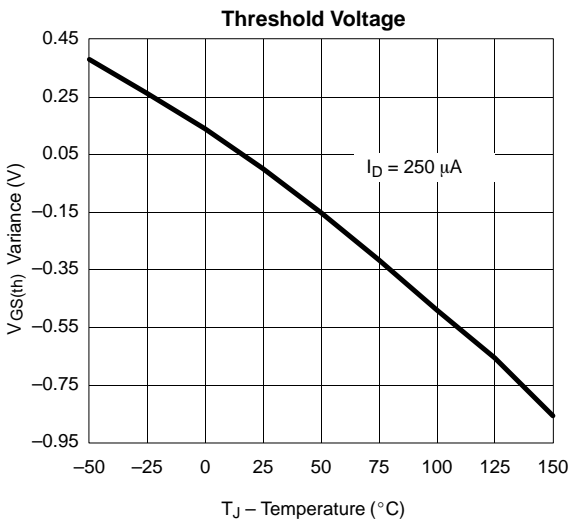
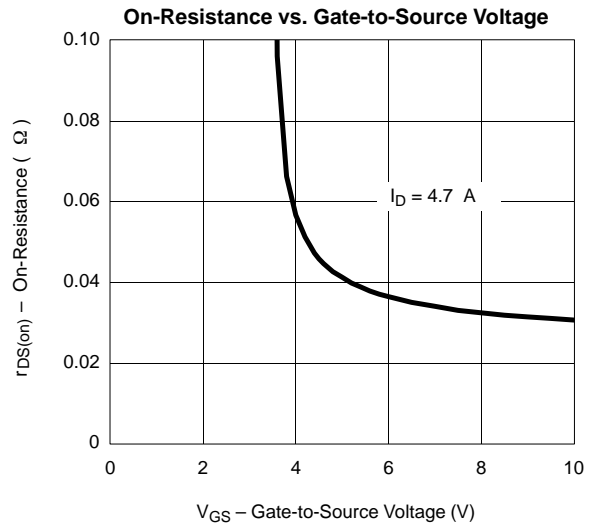
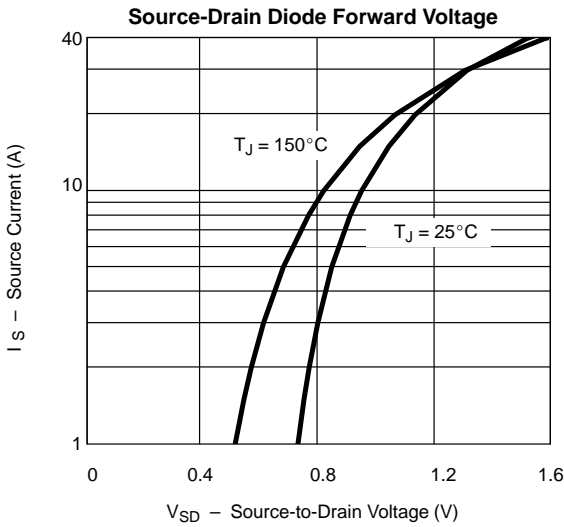


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL 1



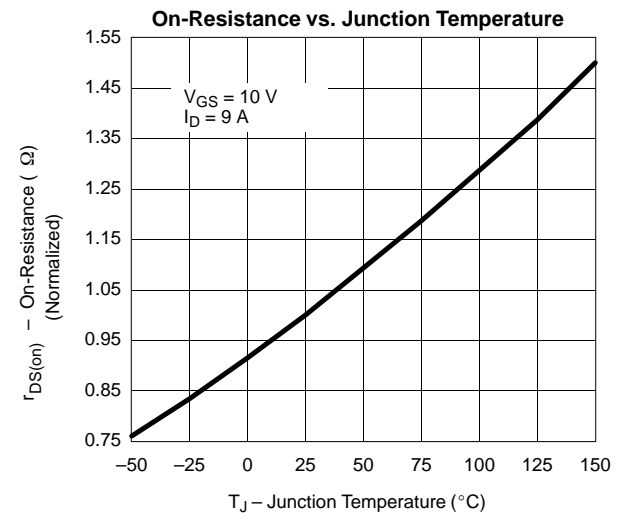
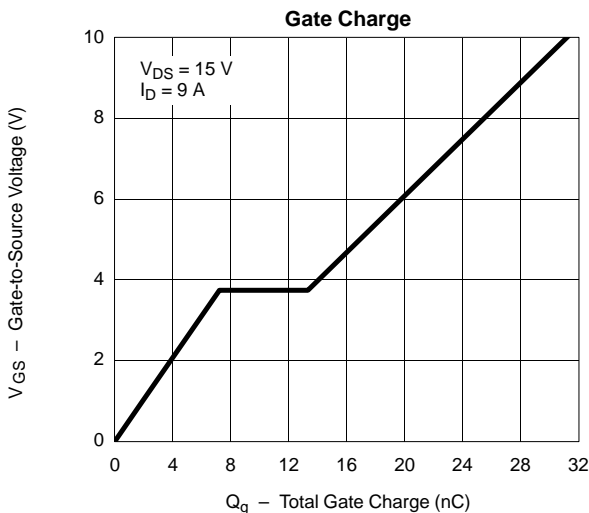
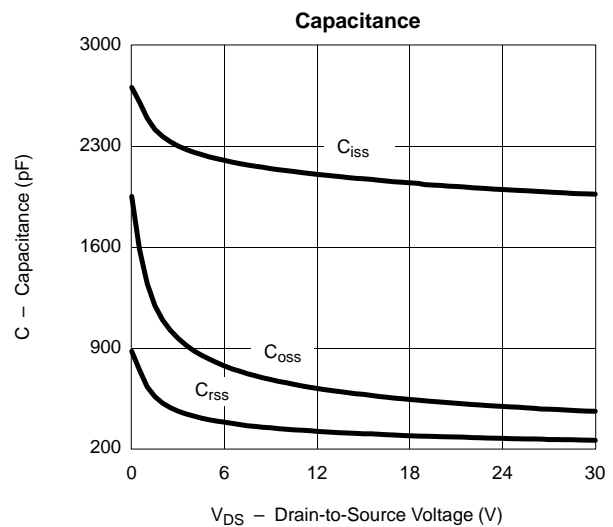
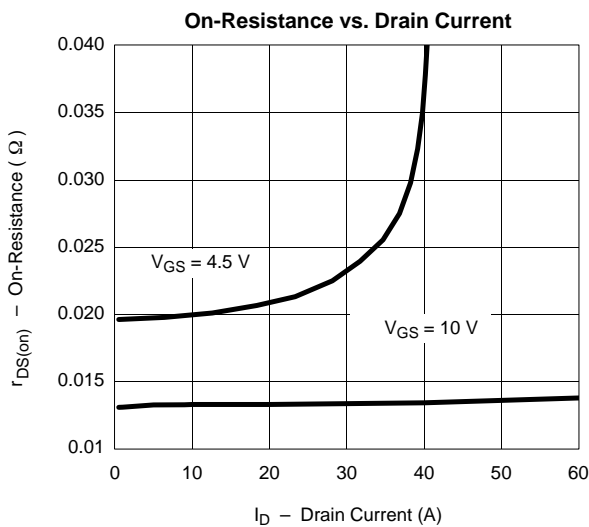
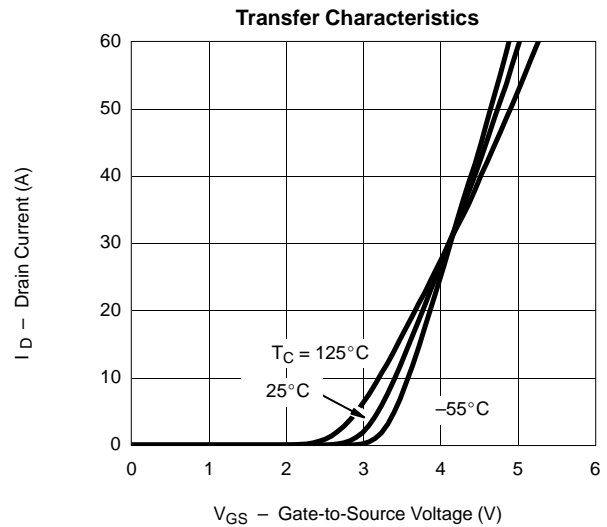
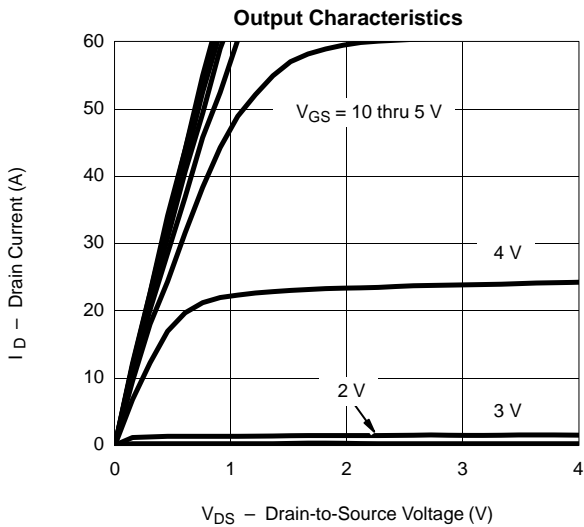
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL 1





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL 2



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL 2

